UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,585	01/18/2005	Jean-Paul Theis		2779

7590 11/29/2007

Pearl Cohen Zedek Latzer LLP
10 Rockefeller Plaza
Suite 1001
New York, NY 10020

EXAMINER	
FAHERTY, COREY S	
ART UNIT	**PAPER NUMBER**
2183	

MAIL DATE	DELIVERY MODE
11/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,585	THEIS, JEAN-PAUL	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *1-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 have been examined.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the complete subject matter of claims 1-12 must be shown or the claims will be cancelled. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

Claim Objections

4. Claims 1-12 are objected to for failing to meet the following requirements: all claims must begin with a capital letter, end with a period, and must contain only one sentence. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 1-2 and 5-12 recite the limitation "and/or", the meaning of which is not clear in the context of claim language. For the purpose of examination, the broadest interpretation of the phrase, "or", will be used.

8. Claims 1 and 2 recite the limitation "the symbolic machine" on page 43, line 26 and page 47, line 3, respectively. There is insufficient antecedent basis for this limitation in the claims.

9. Claims 1 and 2 recite the limitation "one or more data caches at different memory hierarchy levels" in line 5. It is not clear what it means for a single data cache to exist at different memory hierarchy levels. Appropriate correction or clarification is required.

10. Claim 2 recites the limitation "determine a program counter value which is associated with said region (R2) determine which part of the information (IF7) to (IF11) is common both to said region (R2) and to a region other than region (R2)" in lines 18-20 of page 49. The meaning of this phrase is not clear and leaves the scope of the claim indefinite.

11. Claim 4 recites the limitation "said region (R1)" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1-4 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson et al. (*Computer Organization and Design: The Hardware/Software Interface*), referenced from here forward as Patterson, in view of Yeh et al. (*Alternative Implementations of Two-Level Adaptive Branch Prediction*), referenced from here forward as Yeh.

15. Regarding claims 1 and 2, Patterson discloses a method for executing structured symbolic machine code on a microprocessor [page 111, paragraph 4; the binary contents of instructions represent logical processor entities such as registers and addresses in memory], wherein said microprocessor is part of a data processing system containing a memory system [page 111, paragraph 4; page 541, paragraph 2; the computer contains a memory system], where said memory system is defined to have a memory hierarchy [page 541, paragraph 2; the memory system is implemented as a memory hierarchy] containing a register file [page 512, Figure 6.58; the processor contains a register file], a data cache [page 541, paragraph 3; the processor includes a cache implemented using SRAM], and a main memory [page 541, paragraph 3; the processor contains a main memory implemented using DRAM], where said microprocessor has an instruction set containing one or more instructions of which an operand may specify a symbolic variable [page 111, paragraph 4; the binary contents of instructions represent logical processor entities such as registers and addresses in memory], where said structured symbolic machine code contains one or more regions [page 118; instructions contain multiple fields], where one of said regions contains symbolic machine code containing information, where said information contains a symbolic constant of said region and the value of the said symbolic constant [page 118, paragraph 6; the *I-type* instruction, used by data transfer instructions, contains an *address* field for specifying with an immediate, or constant, the address in memory

that will be accessed], where said information may be stored into a memory [page 512, Figure 6.58; instructions may be stored in an instruction memory], where the symbolic machine code contained in each of said regions contains an instruction of which one operand specifies a symbolic variable [page 118, paragraph 6; the *address* field of an *I-type* instruction represents the address at which the memory hierarchy will be accessed], where the symbolic variable specifies one or more entries of a memory other than a register file of said microprocessor [page 118, paragraph 6; the *address* field of an *I-type* instruction represents the address at which the memory hierarchy will be accessed], where said entries are used by the microprocessor in order to determine the addresses within the memory hierarchy where the values of said symbolic variables may be stored to or loaded from during execution of said structured symbolic machine code [page 118; when a memory access instruction is executed, the *address* field is used to determine the address at which the memory hierarchy will be accessed].

Patterson does not explicitly disclose that the microprocessor is able to perform speculative branch prediction, where said speculative branch prediction is based on a branch history which may store outcomes of branches which are not yet resolved at the point in time when a branch prediction is being made, where unresolved branch outcomes may update counter states within the branch history, and where said counter states may concern counter states stored in a pattern history table.

Yeh discloses a microprocessor that is able to perform speculative branch prediction [abstract], where said speculative branch prediction is based on a branch history which may store outcomes of branches which are not yet resolved at the point in time when a branch prediction is being made [page 127, section 3.1, paragraph 2; the branch history is updated speculatively

before the results of the branch are known], where unresolved branch outcomes may update counter states within the branch history [page 126, second column, lines 5-11; a branch history counter is updated using the predicted results of branch instructions]. Yeh teaches that using a branch predictor increases the performance of a processor [abstract] and that speculatively updating branch history counters can increase the accuracy of the predictor [page 127, section 3.1, paragraph 2], resulting in a further increase in processor performance.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to perform speculative branch prediction using speculatively updated branch history counters in the processor of Patterson because Yeh discloses such a branch predictor and teaches that it can improve the performance of a processor [abstract; page 127, section 3.1, paragraph 2].

16. Regarding claim 3, Patterson in view of Yeh discloses a method as claimed in claim 1, wherein one of said regions contains symbolic machine code containing information, where said information contains a symbolic constant of said region and the value of the said symbolic constant [Patterson, page 118, paragraph 6; the *I-type* instruction, used by data transfer instructions, contains an *address* field for specifying with an immediate, or constant, the address in memory that will be accessed], wherein the same one of said regions contains a symbolic variable of said region [page 118, paragraph 6; the *I-type* instruction contains an *opcode* field to indicate that it is of the *I-type* format] as well as a label specifying a dependence group which the symbolic variable pertains to [page 118, paragraphs 1-2, 6; the instruction contains a *rs* field that is used to specify the address that the instruction is dependent on].

17. Regarding claim 4, Patterson in view of Yeh discloses a method as claimed in claim 2, wherein one of said regions contains symbolic machine code containing information, where said

information contains a symbolic constant of said region and the value of the said symbolic constant [Patterson, page 118, paragraph 6; the *I-type* instruction, used by data transfer instructions, contains an *address* field for specifying with an immediate, or constant, the address in memory that will be accessed], wherein the same one of said regions contains a symbolic variable [page 118, paragraphs 1-2, 6; the instruction contains an *opcode* field to indicate that it is of the *I-type* format] that is used to determine one or more labels specifying each a dependence group which the symbolic variable pertains to [page 118, paragraphs 1-2, 6; the instruction contains a *rs* field that is used to specify the address that the instruction is dependent on].

18. Regarding claims 7-10, Patterson in view of Yeh discloses the claimed subject matter. Claims 7-10 recite numerous characteristics that the microprocessor and the instructions of the microprocessor *may* have. As is indicated by the difference between claim 1, which states "where said region (R1) may further contain one or more of the following information: information (IF3)" ... "information (IF6)", and claim 3, which depends on claim 1 and states "where said region (R1) further contains one or more of the following information: information (IF3)" ... "information (IF6)". The only difference between the two limitations is that claim 1 states "may further contain" where claim 3 states "further contains". It is clear from this example that Applicant intends for the modifier "may" to indicate that it is possible for any subsequent limitations to exist in the system, but they do not necessarily *have* to exist. If this were not the case, claim 3 (and claim 4, for similar reasons) would be an improper dependent claim for failing to further limit claim 1. Using this interpretation, the subject matter of claims 7-10 does not require any of the limitations regarding the microprocessor or the instructions, but rather only requires that the limitations be possible. Because there is no evidence in either

Patterson or Yeh that precludes the inclusion of the claimed subject matter in the processor of Patterson in view of Yeh, such a processor reads on claims 7-10.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. The cited references are relate closely to the subject matter of the present application and should be fully considered in any response to this Office Action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Corey S Faherty
Examiner
Art Unit 2183

CF

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100